REMARKS

The Final Office Action mailed May 14, 2009 has been carefully studied and considered. Applicant respectfully traverses all claim rejections for the reasons given below.

35 U.S.C. § 112, First Paragraph Claim Rejections

Claims 1-10 stand rejected under 35 U.S.C. § 112, first paragraph for allegedly failing to comply with the enablement requirement. Applicant respectfully traverses these claim rejections.

Claim features can be **described anywhere** in the specification, including the **drawings**, background and prior art references identified in the specification to satisfy the written description and enablement requirements mandated in the first paragraph of § 112. See *Vas-Cath Inc. v. Mahurkar*, 935 F.2d 1555, 1565 (Fed. Cir. 1991). In the interest of moving prosecution forward in an expedient and proactive manner, the pending claims are listed below along with a corresponding description from the drawings and/or specification satisfying the written description and enablement requirements of § 112.

With regard to claim 1, Figure 2 of the instant application is reproduced immediately below with annotations to show certain aspects of the claimed invention. Figure 2 shows a line driver (3) having output terminals connected to a load (ZL) for supplying a transmit signal to the load ZL and a line receiver (2) having input terminals connected to the load ZL for simultaneously receiving a receive signal from the load ZL as claimed. Figure 2 further shows an arrangement (resistor bridge R1, R2) for canceling the transmit signal on the input terminals of the line receiver 2 as claimed (see also paragraph [0013] of the published application in support). Figure 2 further illustrates the output terminals of the line driver 3 being connected to the load ZL via equal first impedances (ZS) and the input terminals of the line receiver 2 being connected to the load ZL via equal first resistors (R1) and to respective ones of the line driver output terminals via equal second resistors (R2) as recited in claim 1.

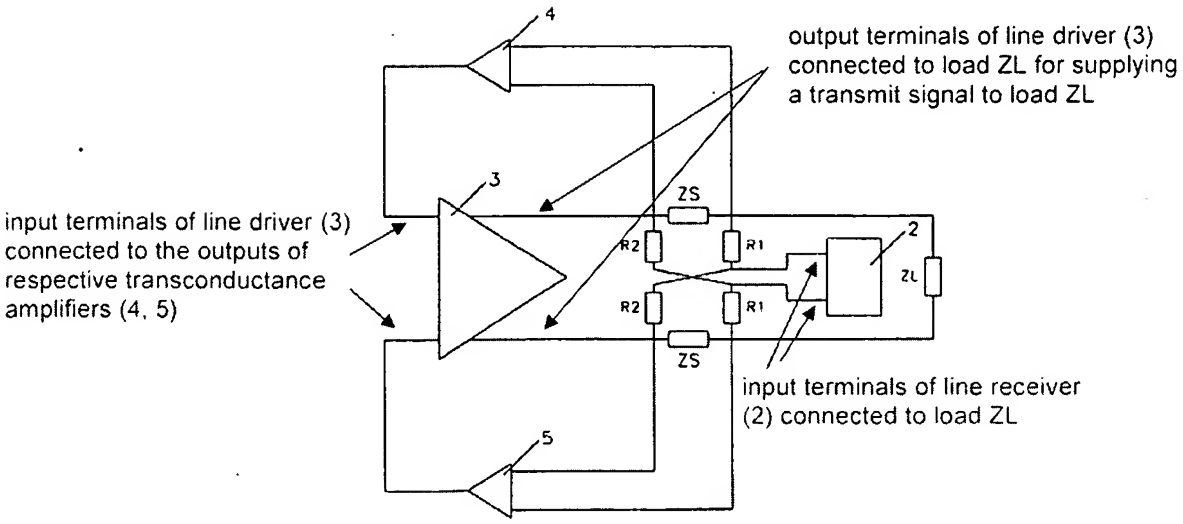


Figure 2 uses the notation 'Z' to denote that the first impedances 'ZS' can be complex as claimed. In further support, paragraph [0028] of the published application states that the first impedances ZS can be complex. Paragraph [0028] also states that the first impedances ZS can be of an impedance value that is much smaller than an impedance value of the load ZL as recited in claim 1.

The Examiner argues that claim 1 recites that the "first impedances are complex impedances to match the load impedance." See p. 4 of the Office Acton. Applicant respectfully disagrees. Claim 1 does not state that the first impedances match the load impedance. Instead, claim 1 recites that the value of the first impedances are much smaller than an impedance value of the load **so that a drive/termination impedance of the line driver matches the load impedance**. Thus, the matching referred to in the specification is with reference to the drive/termination impedance of the line driver, which includes the impedances ZS. Accordingly, it is the drive/termination impedance of the line driver that matches the load impedance according to claim 1, not the first impedances that match the load as suggested by the Examiner.

Paragraph [0031] of the published application states that the drive/termination impedance of the line driver equals kxZS, where k is a gain-related function and ZS represents the impedance value of the claimed first impedances. Thus, the drive/termination impedance of the line driver is a function of both gain and the value of the impedances ZS. As such, the drive/termination impedance of the line driver 3 can be matched to the load when kxZS=ZL as claimed.

The Examiner also argues that without "concrete examples or values or specific implementations", one skilled in the art would not understand the claimed relationship. Applicant respectfully disagrees. As explained above, paragraph [0031] of the published application makes explicitly clear what the claimed relationship is between the different impedances. According to paragraph [0031], the drive/termination impedance of the line driver equals kxZS and can be matched to the load when kxZS=ZL. Since the relationship between the different impedances is a function of gain (of both the line driver 3 and transconductance amplifiers 4 and 5) and the value of the impedances ZS, no specific examples or values can make any more clear that which is already explicitly and unequivocally understandable in the specification. In fact, the last sentence of paragraph [0031] states that any combination of k and ZS that fulfills the equation can be chosen. Thus, the inventors of the present claimed invention clearly envisioned a multitude of different gain and impedance values that would permit the drive/termination impedance of the line driver to match the load.

The Examiner further argues that there is no way one skilled in the art could determine what the relative size (i.e., "much smaller") would be as recited in claim 1. Applicant again respectfully disagrees. Based on the formula given in paragraph [0031] of the instant application, one skilled in the art readily knows that the claim term "much smaller" can mean approximately the load impedance (ZL) divided by the gain factor k, i.e., ZS=ZL/k. Thus, the

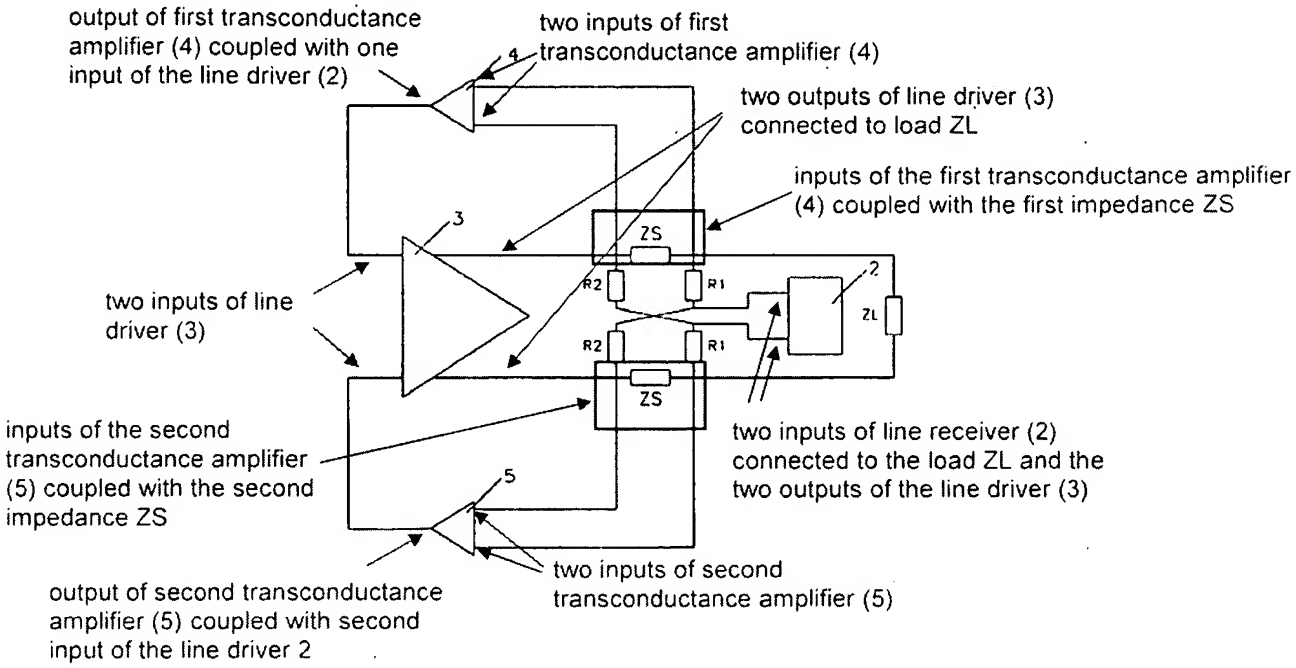
claim term "much smaller" means about 1/kth the load impedance according to the equation given in paragraph [0031].

Figure 2 also shows the claimed transconductance amplifiers (4 and 5) being provided to sense the voltage across the first impedances ZS and supply corresponding currents to respective ones of the line driver input terminals as claimed. Thus, each feature of claim 1 is adequately described in the instant application in such a way as to enable one skilled in the art to practice the claimed invention as required in the first paragraph of § 112.

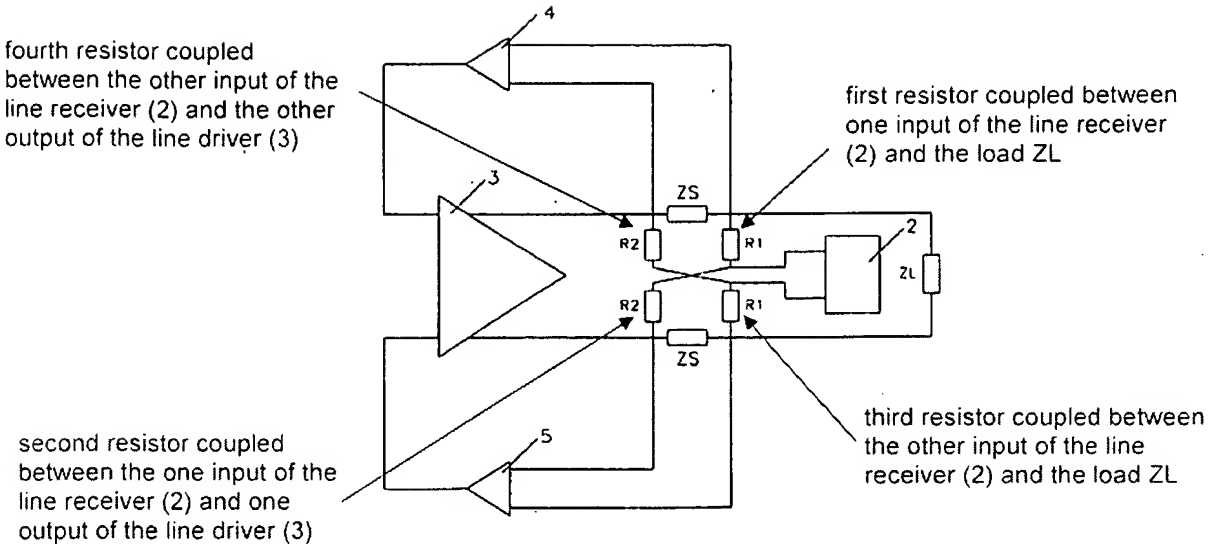
With regard to claim 2, paragraph [0021] of the published application states that "a drive/termination impedance of the line driver may equal the impedance value of one of the impedances multiplied by k, wherein k is a function of the line driver gain and the transconductance amplifier gains" as recited in claim 2. As explained above in careful detail, there is nothing indeterminate about the impedance relationship claimed in claim 2.

With regard to claim 3, Figure 2 of the instant application is reproduced immediately below with annotations to show a line driver (3) having two inputs and two outputs and a load (ZL) coupled with the outputs of the line driver via first and second impedances (ZS) as claimed. Figure 2 also shows a line receiver (2) having two inputs coupled through a network (resistor bridge R1, R2) with the load ZL and the outputs of the line driver 2 as claimed (see also paragraph [0013] of the published application). In addition, Figure 2 shows first and second transconductance amplifiers (4 and 5) having two inputs and an output as recited in claim 3. Figure 2 shows the inputs of the first transconductance amplifier 4 coupled with the first impedance ZS and its output with one input of the line driver 2 and the inputs of the second transconductance amplifier 5 coupled with the second impedance ZS and its output with the other input of the line driver 2 as claimed. Paragraphs [0021], [0028] and [0031] of the published application describes how the first and second impedances ZS can be complex impedances of an impedance value that is much smaller than an impedance value of the load

ZL so that a drive/termination impedance of the line driver 2 matches the load impedance ZL as claimed.



With regard to claim 4, Figure 2 of the instant application is reproduced immediately below with annotations to show the claimed network including a first resistor (first instance of R1) coupled between one input of the line receiver 2 and the load ZL and a second resistor (first instance of resistor R2) coupled between the one input and one output of the line driver as claimed. Figure 2 also shows a third resistor (second instance of R1) of the network coupled between the other input of the line receiver and the load and a fourth resistor (second instance of R2) of the network coupled between the other input and the other output of the line driver as recited in claim 4 (see also paragraph [0021] of the published application).



With regard to claim 5, paragraphs [0021] and [0027] describe how the first and third resistors can be equal and the second and fourth resistors can be equal. With regard to claim 6, see the discussion above regarding dependent claim 2.

Claims 7-10 are similar to claims 3-6 except that the claimed driver is an ADSL driver and the claimed receiver is an ADSL receiver. This language was included in the original claims, and is thus part of the original application. Accordingly, the enablement requirement is satisfied with regard to claims 7-10 at least for the same reasons as claims 3-6.

If the § 112, first paragraph claim rejections are maintained by the Patent Office, Applicant respectfully requests the Examiner to address each piece of evidentiary support submitted herein proving that the enablement requirement is satisfied regarding the subject matter of each pending claim.

35 U.S.C. § 112, Second Paragraph Claim Rejections

Claims 1-10 stand rejected under 35 U.S.C. § 112, second paragraph for allegedly being indefinite. Applicant respectfully traverses these claim rejections.

Particularly, the Examiner argues that it is unclear as to what is meant by the claim term "much smaller" because there are no examples or values disclosed. As explained above, the formula given in paragraph [0031] of the instant application makes clear that the claim term "much smaller" can mean approximately the load impedance (ZL) divided by the gain factor k, i.e., ZS=ZL/k. Thus, the claim term "much smaller" means about 1/kth the load impedance according to the equation given in paragraph [0031]. There is nothing indefinite about this claim term in the context of the present claimed invention.

Drawing Objection

The drawings still remain objected to. The Examiner argues that "the means for coupling the claimed 'transmit signal' along with the claimed input terminals receiving the signals from the transconductance stages" must be shown in the drawings. As explained in the prior office action response filed on February 23, 2009, Figure 2 of the instant application shows the output terminals of the line driver (3) connected to the load (ZL) for supplying a transmit signal to the load. The transmit signal is a signal. It is unclear how the actual signal is to be shown in a circuit-level diagram. It is well known that conductors such as those shown in Figure 2 connecting the output terminals of the line driver (3) to the load (ZL) can carry a signal from one point (e.g., the line driver output terminals) to another point (e.g., the load). Such a conventional and basic feature such as the transmission of a signal over a conductor need not be shown in the Figures.

Figure 2 also shows the input terminals of the line driver (3) being connected to the outputs of respective transconductance amplifiers (4, 5) so that the line driver can receive signals from the transconductance amplifiers. Again, the actual signals carried over the claimed connections need not be shown in the Figures for the reasons given above. Figure 2 adequately shows all claimed circuit connections. As such, Applicant respectfully requests withdrawal of the drawing objections.

Conclusion

In view of the remarks made herein, Applicant respectfully submits that the present application is in condition for immediate allowance. Action to such affect is respectfully requested. The Examiner is encouraged to contact Applicants' attorney at (919)-854-1844 if any outstanding matters can be readily addressed by a phone call.

Respectfully submitted,

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